REMARKS

1. Claims 17 and 18 are objected to under 37 CFR 175 (c) and claim 17 is amended in response to this rejection.

2. Claims 1-7, 16-19 and 27 are rejected under 35 USC 102(b) as being unpatentable over U.S. patent number 5,684,482 (GALTON). The Examiner is respectfully requested to withdraw the rejection of this claims for the reasons discussed below.

Claim 1

A dynamic encoder formed by a tree of switching blocks converts a binary encoded input word that may have any value from 0-n into an n-bit output word, where the number of bits of the output word that are a 1 is equal to the value of the input word. In a conventional dynamic encoder such as taught by GALTON, each switching block 120-126 (FIG. 2) is a "Radix-2" encoder, meaning that it converts each input word into two (R = 2) output words. An encoder using only Radix-2 switching blocks requires a tree having log (n) layers of switching blocks. In the example of GALTON's FIG. 2, three layers of switching block are required to convert an input word x [n}of value 0-8 into eight output bits y_1-y_8. The maximum allowable frequency of operation of the dynamic encoder decreases with the number of layers in the switching block tree. See the applicant's specification paragraph 0038.

The invention recited in claim 1 reduces the number of layers of switching blocks needed in a dynamic encoder by using at least one switching block that produces more than two output words in response to its input work. For example, in the applicant's FIG. 8, two of the switching blocks (S1,1 and S1,2) are Radix-4 switching blocks (R=4), meaning that they produce four output words in response to each input word. This enables the applicant's 8-bit dynamic encoder of FIG. 8 to use only two

layers of switching blocks rather than three as in GALTON's FIG. 2. This allows the applicant's 8-bit encoder of FIG. 8 to have a higher operating frequency than GALTON's 8-bit encoder of FIG. 2.

In particular, claim 1 recites, "A dynamic encoder … comprising a plurality of switching blocks … wherein each switching block receives a block input word and converts in into R block output words … wherein for at least one of the plurality of switching blocks R>2."

The Examiner cites GALTON FIG. 2 as showing a dynamic encoder in which at least one switching block has more than two output words (R>2), but each switching block in GALTON's FIG. 2 produces only R = 2 output words; none of the switching blocks produces R>2 output words as recited in the applicant's claim 1. In particular,

- GALTON's switching block 120 receives one input word and produces only R=2 two output words 140 and 141,
- GALTON's switching block 121 receives one input word and produces only R=2 two output words 144 and 145,
- GALTON's switching block 122 receives one input word and produces only R=2 two output words 146 and 147,
- GALTON's switching block 123 receives one input word and produces only R=2 two output words 152 and 153,
- GALTON's switching block 124 receives one input word and produces only R=2 two output words 154 and 155,
- GALTON's switching block 125 receives one input word and produces only R=2 two output words 156 and 157,
- GALTON's switching block 126 receives one input word and produces only R=2 two output words 158 and 159

See also GALTON, col. 2, lines 45-49 and col. 12 (claim 1) line 45-46.

Claim 1 is therefore patentable over GALTON because GALTON fails to disclose or suggest the use of R>2 switching blocks in a dynamic encoder.

Claim 2

Claim 2 depends on claim 1 and is patentable over GALTON for similar reasons. Claim 2 is further patentable over GALTON because it recites that for every switching block of every layer of the tree is other than the highest layer of the tree R>2. R is not greater than 2 for any of GALTON's switching blocks .

Claim 3

Claim 3 depends on claim 1 and is patentable over GALTON for similar reasons. Claim 3 is further patentable over GALTON because it recites that R=4 for at least one switching block.. R = 2 for all of GALTON's switching blocks .

Claim 4

Claim 4 depends on claim 3 and is patentable over GALTON for similar reasons. Claim 4 is further patentable over GALTON because it recites that R=4 for at every switching block.. R = 2 for all of GALTON's switching blocks .

Claim 5

Claim 5 depends on claim 1 and is patentable over GALTON for similar reasons. Claim 5 is further patentable over GALTON because it recites that R differs for at least two switching blocks. R = 2 for all of GALTON's switching blocks

Claim 6

Claim 6 depends on claim 1 and is patentable over GALTON for similar reasons. Claim 6 is further patentable over GALTON because it recites that R is other than a power of two for at

least one switching block.. R is a power of 2 for all of GALTON's switching blocks.

Claim 16

Claim 16 recites a method for generating an N-bit encoded output word in response to each encoder input word that includes a step (a) of converting each encoder input into a set of M generated words, a step (b) of converting each generated word into a separate set of R generated words, and a step (c) of repeating step (b) until all generated words comprise only a single bit, "where for at least one execution of step b, R>2."

The Examiner cites GALTON FIG. 2 as inherently carrying out such a method, however in no case is any generated word converted in any one step to a set of four words. Thus for all conversion steps R=2 and for no conversion step is R>2.

Claim 17

Claim 17 (as amended) depends on claim 16 and is patentable over GALTON for similar reasons.

Claim 18

Claim 18 depends on claim 17 and is patentable over GALTON for similar reasons. Claim 18 is further patentable over GALTON because it recites that M = 4. For GALTON's FIG. 2, M = 2 since the first layer switching block 120 produces two output words 140-141.

Claim 19

Claim 19 depends on claim 18 and is patentable over GALTON for similar reasons. Claim 19 is further patentable over GALTON because it recites that R=4 during each execution of step b. Every switching block carries out a step of converting an input word into R = 2 output words; none produce R = four output words.

Claim 27

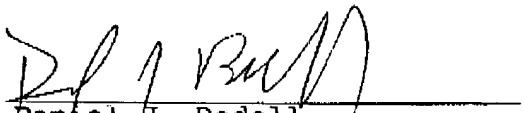
Claim 27 recites, "A dynamic digital-to-analog converter (DAC) ... comprising ... a plurality of switching blocks ... wherein each switching block receives a block input word and converts in into R block output words ... wherein for at least one of the plurality of switching blocks R>2."

The Examiner cites GALTON FIG. 2 as showing a dynamic encoder in which at least one switching block has more than two output words (R>2), but each switching block in GALTON's FIG. 2 produces only R = 2 output words; none of the switching blocks produces R>2 output words as recited in the applicant's claim 1. Thus claim 27 is patentable over GALTON.

4. The Examiner objected to claims 8-15, 20-26 and 28-33 as being dependant upon rejected base claims. In view of the forgoing discussion distinguishing the base claims over the prior art, it is believed that the base claims are patentable. The Examiner is therefore respectfully requested to withdraw the objections to these claims.

In view of the foregoing amendments and remarks it is believed the application is in condition for allowance. Notice of Allowance is therefore respectfully requested.

Respectfully submitted,



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